IN THE CLAIMS

1. (currently amended) A semiconductor device comprising:

a silicon substrate constituting a base;

a semiconductor chip provided on said base and having a first main surface on which a plurality of electrode pads is provided, a surface ~~protecting~~ protection film formed on said first main surface such that said electrode pads are exposed, a second main surface which opposes said first main surface, and a plurality of side surfaces between the surface of said surface ~~protecting~~ protection film and said second main surface;

an insulating extension portion formed on said base so as to surround said side surfaces of said semiconductor chip;

a plurality of wiring patterns electrically connected to said electrode pads and extended from said electrode pads to the surface of said extension portion;

a plurality of electrode posts formed on portions of said wiring patterns, the portions of said wiring patterns being arranged on the insulating extension portion;

a sealing ~~portion~~ resin formed on said wiring patterns, said insulating extension potion, and the side surfaces of the electrode posts; ~~such that a part of each of said wiring patterns is exposed;~~ and

a plurality of external terminals provided ~~over said wiring patterns in a region including the upper side of said extension portion~~ on said electrode posts.

2. (canceled)

3. (original): The semiconductor device according to claim 2, wherein said electrode posts are formed from a conductive material.

4. (canceled)

5. (original): The semiconductor device according to claim 1, wherein said external terminals are formed as solder balls.

6. (original): The semiconductor device according to claim 1, wherein portions of the wiring patterns on a boundary and vicinity thereof between semiconductor chip and the extension portion are formed wider or more thickly than other portions of said wiring patterns.

7. (original): The semiconductor device according to claim 1, wherein said extension portion is formed from an insulating material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

8. (original): The semiconductor device according to claim 7, wherein said extension portion is formed from an insulating liquid resin having a linear expansion coefficient in a temperature range than glass transition point of less than 1.5×10^{-5}/°C and a modulus of elasticity within a range of 7.8 to 22 GPa.

9. (currently amended) A semiconductor device comprising:

a silicon substrate constituting a base;

an extension portion having a concave portion which is formed from an insulating material and provided on said base;

a semiconductor chip having a first main surface on which a plurality of electrode pads are provided, a surface ~~protecting~~ protection film formed on said first main surface such that said electrode pads are exposed, a second main surface which opposes said first main surface, and a plurality of side surfaces between the surface of said surface ~~protecting~~ protection film and said second main surface, which is provided within the concave portion of said extension portion such that said side surfaces are surrounded by said extension portion;

a plurality of wiring patterns electrically connected to ~~each of~~ said electrode pads and extended from said electrode pads to the surface of said extension portion;

a plurality of electrode posts formed on portions of said wiring patterns, the portions of said wiring patterns being arranged on the extension portion;

a sealing ~~portion~~ resin formed on said wiring patterns, said extension potion, and the side surfaces of the electrode posts; ~~such that a part of each of said wiring patterns is exposed;~~ and

a plurality of external terminals provided on said electrode posts. ~~wiring patterns in a region including the upper side of said extension portion.~~

10. (canceled)

11. (original): The semiconductor device according to claim 10, wherein said electrode posts are formed from a conductive material.

12. (canceled)

13. (original): The semiconductor device according to claim 9, wherein portions of the wiring patterns on a boundary and vicinity thereof between semiconductor chip and the extension portion are formed wider or more thickly than other portions of said wiring patterns.

14. (original): The semiconductor device according to claim 9, wherein said extension portion is formed from an insulating material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

15. (original): The semiconductor device according to claim 14, wherein said extension portion is formed from an insulating liquid resin having a linear expansion coefficient in a lower

temperature range than glass transition point of less than 1.5×10^{-5}/°C and a modulus of elasticity within a range of 7.8 to 22 GPa.

16. (currently amended) A semiconductor device comprising:

a silicon substrate constituting a base;

an insulating extension portion provided on said base and having a concave portion having inclined inside walls;

a semiconductor chip comprising a first main surface on which a plurality of electrode pads is provided, a surface protecting film formed on said first main surface such that said electrode pads are exposed, a second main surface which opposes said first main surface, and a plurality of side surfaces between the surface of said surface protecting film and said second main surface, which is provided within the concave portion of said extension portion such that said side surfaces are surrounded by said extension portion;

an insulating film formed over the surface of said inside walls, the surface of said extension portion, and said surface protecting film such that a part of said electrode pads is exposed;

a plurality of wiring patterns formed on said insulating film, electrically connected to said electrode pads, and extended from said electrode pads to the surface of said extension portion;

a plurality of electrode posts formed on portions of said wiring patterns, the portions of said wiring patterns being arranged on the insulating extension portion;

a sealing ~~portion~~ resin formed on said wiring patterns, said insulating extension potion, and the side surfaces of the electrode posts; ~~such that a part of each of said wiring patterns is exposed;~~ and

a plurality of external terminals provided ~~over said wiring patterns in a region including the upper side of said extension portion~~ on said electrode posts.

17.-18. (canceled)

19. (original): The semiconductor device according to claim 16, wherein said extension portion is formed from an insulating material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

20. (original): The semiconductor device according to claim 19, wherein said extension portion is formed from an insulating liquid resin having a linear expansion coefficient in a lower temperature range than glass transition point of less than $1.5 \times 10^{-5}/°C$ and a modulus of elasticity within a range of 7.8 to 22 GPa.

21. (previously presented): The semiconductor device according to claim 1, wherein said semiconductor chip is in contact with said silicon substrate.

22. (previously presented): The semiconductor device according to claim 9, wherein said extension portion is in contact with said silicon substrate.

23. (previously presented): The semiconductor device according to claim 16, wherein said insulating extension is in contact with said silicon substrate.

Kato does not disclose the features of amended claims 1, 9 and 16, and does not attain the above-mentioned advantageous effects.

[3] Claims 7, 8, 14, 15, 19 and 20 were rejected under §103 over Park '259 in view of Tokuda '289 and Kato '764 and Yamaguchi JP '354. This rejection is respectfully traversed on the grounds set out above.

[4-5] Claims 1-3, 6-11, 13-17, 19 and 20 were rejected over claims of 10/722,446 in view of Kato for obviousness-type double patenting. This rejection is respectfully traversed.

First, the rejection is believed to be improper because it applies an outside reference (i.e., Kato). No support for this is seen in the MPEP and it is respectfully submitted to be contrary to the whole idea of a double patenting rejection, which is a rejection of claims over claims. If outside references can be brought in without limit, then the double patenting rejection is no different from any §103 rejection, except that any co-assigned application (which maybe is not prior art) can be applied, too.

Second, the Examiner asserts that it would have been obvious to use a silicon base for heat dissipation, but the claims of 10/722,446 do not mention heat dissipation. The reference's claim 1 already recites a base that is "capable of conducting heat [from the chip] into the atmosphere," so this reference does not suggest any need for better heat conduction. Conversely, Kato, in the cited text at the top of column 19, teaches that the substrate can be eliminated altogether (at line 9). Kato is not seen to teach toward a heat-dissipating base.

The Applicant previously argued that reference 10/722,446 was filed on November 28, 2003, after this application was filed, so MPEP §804(B)(1)(b) applies, but the Examiner had not indicated that the questions of administrative delay and the possibility of the Applicant filing simultaneously with 10/722,446 were considered. The Examiner traverses this argument but does not explain.

[6] Claims 1-3, 5 and 8 were rejected over the claims of 10/697,247 for obviousness-type double patenting. This rejection is respectfully traversed on the basis of the arguments above.